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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,222	09/04/2001	Yongping Fan	2207/11986	2631

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,222	FAN ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *25 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,18 and 26-35* is/are pending in the application.

4a) Of the above claim(s) *10 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,26-28 and 30-35* is/are rejected.

7)☒ Claim(s) *29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 10 and 18 were withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species in the actions of 12/28/04 and 3/31/05. It is noted that as amended, claims 1 is generic for claims 10 and 18.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 8, 27, 28, and 30-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The specification, drawings, and originally filed claims are silent as to the presence of an "output lead," a "bias lead," or a "power lead." Instead, the disclosure only depicts power, bias, and output terminals.

For the purposes of examination, it is assumed that the claimed output, bias, and power leads refer to the disclosed output, bias, and power terminals.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 7, 8, 31, and 32are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,821,768 to Rau.

Regarding claim 1, Rau discloses a termination resistor comprising: a first transistor (figure 4 – upper right transistor); a second transistor (upper center transistor) having a gate coupled to a gate of the first transistor and a drain coupled to a drain of the first transistor (gates and drains are directly connected – see figure 4); a third transistor ('M3' transistor) having a drain coupled to a source of the second transistor (figure 4 – coupled with a direct connection); and a first resistor (Rref, or alternately, either or R3 or R4) coupled between a source of the first transistor and a gate and source of the third transistor (connected indirectly, through intervening transistor and resistor elements).

Regarding claims 2-4, Rau discloses that the transistors include PMOS and NMOS devices (column 5, lines 30-67).

Regarding claim 7, Rau discloses a differential amplifier (5) having an output coupled with the first and second gates (see figure 4 – coupled through a direct connection), and having a

first input coupled to the first resistor and source and gate of the third transistor (either input is indirectly connected to each of the claimed elements through intervening elements).

Regarding claim 8, Rau discloses a ground terminal coupled to ground ('GND' terminal) and a second resistor (R4) coupled 'between' the first input ('+') and the ground terminal (indirect connection through transistors M3 and M4).

Regarding claims 31 and 32, Rau discloses an output lead (Uout) coupled to the output of the differential amplifier (figure 4 – indirect connection through intervening circuit elements).

6. Claims 1-4 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,388,495 to Roy et al.

Regarding claim 1, Roy discloses a termination resistor (column 1, lines 5-10) comprising: a first transistor (130); a second transistor (135) having a gate coupled to the gate of the first transistor (direct coupling – see figure 6), and having a drain coupled to a drain of the first transistor (indirect connection through resistor 145); a third transistor (140) having a drain coupled to a source of the second transistor (direct connection – see figure 6); and a first resistor (150) coupled between a source of the first transistor and a source (direct connection) and a gate (indirect connection across transistor 140) of the third transistor (figure 6).

Regarding claims 2-4, Roy discloses that the transistors may include NMOS devices (for transistors 130, 135, 140; see column 6, lines 33-35) or PMOS devices connected in a similar manner as the NMOS devices (see figure 6 - devices 165=first transistor, 170=2nd transistor, 175=3rd transistor; column 6, lines 55-57).

Regarding claim 26, Roy discloses that the first resistor is connected between the source of the first transistor and ground. Hence, the first resistor automatically decreases the possible voltage drop across the first transistor and inhibits the ability of the first transistor to go into saturation (see figure 6).

7. Claims 1-4 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,351,138 to Wong.

Regarding claim 1, Wong discloses a termination resistor (column 2, lines 29-30) comprising: a first transistor (28); a second transistor (26) having a gate coupled to a gate of the first transistor (connected across intervening capacitor elements 36 and 38) and a drain coupled to a drain of the first transistor (directly connected – see figure 2); a third transistor (42) having a drain coupled to a source of the second transistor (directly connected); and a first resistor (34) coupled between a source of the first transistor and a source and gate of the third transistor (connected indirectly through intervening capacitor elements and resistor elements 32, 36, and 38).

Regarding claims 2-4, Wong discloses the use of CMOS transistors (column 1, lines 55-67).

Regarding claim 27, Wong discloses a bias terminal connected to a bias voltage and coupled to the gates of the first and second transistors (figure 2 – source voltage – gates coupled through capacitors and resistor 32); a power terminal (trans. Line) coupled to the drains of the first and second transistors); and an output terminal (alternately ground, Vpg, or Vng) coupled to the resistor and gate and source of the third transistor (through indirect connections).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of U.S. Patent No. 6,429,685 to Stockstad.

Wong is silent as to the material nature of the first resistor.

Stockstad discloses a termination circuit wherein the resistors are poly resistors (see column 10, lines 42-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the resistors of Wong are poly resistors, as suggested by Stockstad. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use poly resistors, because Stockstad shows that poly resistors are appropriate for use in termination circuits including resistors and MOS transistors (see Stockstad, column 10, lines 42-55). It would be apparent to a person skilled in the art that using polycrystalline silicon for a resistor would be advantageous over external resistors or other resistor structures, since it could be fabricated together with the MOS transistors, thus reducing the fabrication complexity and need for additional components.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of the IEEE article to Griffin (cited by applicant).

Wong fails to disclose that the first resistor may be formed as a PMOS device.

Griffin discloses that the use of an active resistor, comprising MOS transistors, can provide a high degree of I-V linearity over a large signal range, and additionally, can enable greater integration of a circuit structure (see Griffin, sections II-IV).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the resistor of Wong with the active resistor of Griffin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use an active resistor comprising a MOS structure, because Griffin shows that MOS resistors have good linearity and signal range, such that they are advantageously used as resistors (see Griffin, sections II-IV). Additionally, since the circuit structure of Wong already uses MOS devices, it would be possible to form the resistor structure in the same fabrication steps as the transistor structures, thus decreasing fabrication complexity.

Allowable Subject Matter

11. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for allowability is that the prior art generally teaches the use of plural resistors, each having a relatively small resistance. There is simply no suggestion in the prior art of using a resistor connected as claimed that has a resistance equal to about 50% of the total resistance of the circuit. Furthermore, since the circuit structure appearing in the Applicant's disclosure is significantly different from the structures taught in the prior art, there is no reasonable expectation that the circuits would have similar current-voltage characteristics or operate in a similar manner. Hence, it would not be reasonable to expect that the resistance of the first resistor in the prior art references could be modified such that the resistor has a resistance of about 50% of the total resistance of the circuit without destroying the operability of the circuit.

Response to Arguments

13. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new grounds of rejection.

The Examiner notes that the term "coupled" does not require a direct electrical connection with no intervening elements, but rather only requires that the elements are connected in such a manner that they mutually affect each other. Hence, as long as the elements are located somewhere along a same electrical path, or as long as the elements are disposed such that the presence of one element affects the current or voltage of another element, the elements are considered to be 'coupled.'

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

LAURA M. SCHILLINGER
PRIMARY EXAMINER